IN THE CLAIMS

Amend Claims 8 and 21 and cancel Claims 7, 30, and 33 - 42 without prejudice so that the claims are as follows:

1. (Canceled)

2. (Previously presented) The ESD protection structure of Claim 8, wherein said first conductivity type is n-type, and said second conductivity type is p-type.

3. (Previously presented) The ESD protection structure of Claim 8, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

4. (Canceled)

5. (Previously presented) The ESD protection structure of Claim 8, wherein said third semiconductor region includes a well region of said first conductivity type formed in a semiconductor substrate of said second conductivity type.

6. (Previously presented) The ESD protection structure of Claim 5, wherein each of said second and fourth semiconductor regions includes a base region of said second conductivity type formed in said well region.

7. (Canceled)

8. (Currently amended) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit, said ESD protection structure comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type continuous with said first semiconductor region, said second conductivity type being opposite to said first conductivity type;

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

an electrically floating third semiconductor region of said first conductivity type continuous with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type continuous with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region, each of said second and fourth semiconductor regions comprising a main portion and a contact portion more heavily doped than said main portion;

a fifth semiconductor region of said first conductivity type continuous with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region;

a first terminal connected to said first semiconductor region and to the contact portion of said second semiconductor region; ~~regions;~~

a second terminal connected to said ~~fourth and~~ fifth semiconductor region and to the contact portion of said fourth semiconductor region; ~~regions;~~

a first resistor coupled between said first terminal and said second semiconductor region;

a first current source coupled between said terminals so as to be in series with said first resistor;

a second resistor coupled between said second terminal and said fourth semiconductor region; and

a second current source coupled between said terminals so as to be in series with said second resistor.

9 - 20. (Canceled)

21. (Currently amended) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit, said ESD protection structure, comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type continuous with said first semiconductor region, said second conductivity type being opposite to said first conductivity type;

Ronald J. Meetin
Attorney at Law
210 Central Avenue
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94043-4869
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Fax: 650-964-9779

an electrically floating third semiconductor region of said first conductivity type continuous with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type continuous with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region, each of said second and fourth semiconductor regions comprising a main portion and a contact portion more heavily doped than said main portion;

a fifth semiconductor region of said first conductivity type continuous with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region;

a first terminal connected to said first semiconductor region and to the contact portion of said second semiconductor region; ~~regions;~~

a second terminal connected to said ~~fourth and~~ fifth semiconductor region and to the contact portion of said fourth semiconductor region; ~~regions;~~

a first resistor coupled between said first terminal and said second semiconductor region;

a first pair of back-to-back diodes coupled between said terminals so as to be in series with said first resistor;

a second resistor coupled between said second terminal and said fourth semiconductor region; and

a second pair of back-to-back diodes coupled between said terminals so as to be in series with said second resistor.

22. (Previously presented) The ESD protection structure of Claim 21, wherein said diodes are Zener diodes.

23 - 25. (Canceled)

26. (Previously presented) The ESD protection structure of Claim 21, wherein said first conductivity type is n-type, and said second conductivity type is p-type.

27. (Previously presented) The ESD protection structure of Claim 21, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
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Fax: 650-964-9779

28. (Previously presented) The ESD protection structure of Claim 21, wherein said third semiconductor region includes a well region of said first conductivity type formed in a semiconductor substrate of said second conductivity type.

29. (Previously presented) The ESD protection structure of Claim 28, wherein each of said second and fourth semiconductor regions includes a base region of said second conductivity type formed in said well region.

30. (Canceled)

31. (Previously presented) The ESD protection structure of Claim 8, wherein said first current source is coupled between said second terminal and said second semiconductor region, and said second current source is coupled between said first terminal and said fourth semiconductor region.

32. (Previously presented) The ESD protection structure of Claim 21, wherein said first pair of Zener diodes are coupled between said second terminal and said second semiconductor region, and said second pair of Zener diodes are coupled between said first terminal and said fourth semiconductor region.

33 - 42. (Canceled)

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779